

QUERY CONTROL FORM

RTIS USE ONLY

Application No. 09927276

Prepared by TW

Tracking Number SP93457

Examiner-GAU Ryan-1745

Date 4-23-04

Week Date 1-19-04

No. of queries	Time (s)	Time (s)	Time (s)	Time (s)	Time (s)
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62	0.00	0.00	0.00	0.00	0.00

JACKET

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|----------------------|------------------------|--------------------|----------------|
| a. Serial No. | f. Foreign Priority | k. Print Claim(s) | p. PTO-1449 |
| b. Applicant(s) | g. Disclaimer | l. Print Fig. | q. PTOL-85b |
| c. Continuing Data | h. Microfiche Appendix | m. Searched Column | r. Abstract |
| d. PCT | i. Title | n. PTO-270/328 | s. Sheets/Figs |
| e. Domestic Priority | j. Claims Allowed | o. PTO-892 | t. Other |

SPECIFICATION

- a. Page Missing
- b. Text Continuity
- c. Holes through Data
- d. Other Missing Text
- e. Illegible Text
- f. Duplicate Text
- ☒ g. Brief Description
- h. Sequence Listing
- i. Appendix
- j. Amendments
- k. Other

CLAIMS

- a. Claim(s) Missing
- b. Improper Dependency
- c. Duplicate Numbers
- d. Incorrect Numbering
- e. Index Disagrees
- f. Punctuation
- g. Amendments
- h. Bracketing
- i. Missing Text
- j. Duplicate Text
- k. Other

MESSAGE

The description and Figure for Figure 6 and 11 do not agree.

Described - Figures 6A-6E, Drawings 6A-6C
Described - Figures 11A-11E, Drawings 11A-11C

Please verify

Thank You

initials *TV*

RESPONSE

RESPONSE Typos corrected.

initials

FIG. 4, another embodiment of the present invention, illustrates a means of supplying power to the heat dissipating structure.

FIGS. 5a through 5c one method of fabricating thermoelement couples onto an IC device substrate.

FIGS. 6a through 6^c_A another method of fabricating the present invention.

FIGS. 7a through 7c illustrates a method of manufacture involving wafer bonding of a heat dissipating structure to a IC device.

FIG. 8 illustrates another embodiment of the present invention utilizing wafer bonding.

FIGS. 9a through 9d illustrate an electrical series of dissimilar thermoelements integrated with (or attachable to) an IC device substrate whereby either power is applied to or generated by the structures.

FIGS. 10a through 10c illustrate a closed circuit thermoelectric couple as one embodiment of the present invention.

FIGS. 11a through 11^c_A illustrate a single semiconducting thermoelement with multiple cascaded stages.

FIG. 12 illustrates a CSP electronic component package for housing the silicon substrate in the present invention.

FIG. 13 illustrates a FCMCM electronic component package for housing the silicon substrate in the present invention.

FIG. 14 illustrates a wire-bonded TBGA electronic component package for housing the silicon substrate in the present invention.

FIG. 15 illustrates a FCBGA electronic component package for housing the silicon substrate in the present invention.

35 Best Mode for Carrying Out the Invention

Described below are several embodiments of the present invention which illustrate various ways the present invention can be implemented. In the descriptions that

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